USB 3.1 & Type C™ System Electrical Design

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Agenda

Challenges
• Interoperability & Compliance Testing
• Performance Metrics
• PCB Routing Baseline Estimates
• Type C™ Impacts

Options for Extending PCB Length
• Low Loss PCBs
• Cabled solutions
• Repeaters

Additional Considerations
• Thin PCBs
• PCB Vias
• Connector Footprint Optimization
• Crosstalk Minimization
Challenges

• Interoperability & Compliance
• Key Design Metrics
• PCB Route Length Baseline
• Type C Impacts
USB Usage Model

Any certified host works with any certified hub or device.
USB 3.1 System Design Challenge

- Jitter budget is basis for Tx and Rx compliance specs.
- Loss budget is basis for compliance channels.

Challenge: PCB routing
- Budget includes pad cap, package, PCB
- Also includes muxes (if discrete)
- Practical route length <6”
- Consider a repeater if design exceeds 8.5dB
Transmitter Compliance

Compliance Metrics: 32.9ps eye width @ 1e-12 BER
70mV eye height over $10^6$ UI

Compliance requires Tx meet a minimum eye mask when connected to compliance channel.
Receiver Compliance

• JTOL test connected to 14.5dB compliance channel.
  ▪ Transmit minimum compliant eye at output of reference Rx equalizer.
  ▪ Replace reference EQ (scope) with DUT.
  ▪ Initialize link & train receiver.
  ▪ Measure JTOL.

• Receiver must be at least as capable as the spec reference receiver.

Compliance requires Rx operate with a minimum eye after transmission over compliance channel.
Key Electrical Metrics

Silicon
• Swing
• Jitter
• Equalization

System
• Loss
• Reflections
• Crosstalk

System performance maps to these parameters:
• Loss: Fitted insertion loss @ Nyquist (5GHz)
• Reflections: Integrated multi-reflection noise
• Crosstalk: Integrated crosstalk

Refer to the “USB 3.1 System Design” presentation from November 2015 for details and usage. Available at:
## Key Performance Factors

<table>
<thead>
<tr>
<th></th>
<th><strong>Loss</strong></th>
<th><strong>Reflections</strong></th>
<th><strong>Crosstalk</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon</td>
<td>Jitter</td>
<td>Pad Cap</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Equalization</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Pad Cap</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Package</td>
<td>Stackup</td>
<td>Stackup</td>
<td>Stackup</td>
</tr>
<tr>
<td></td>
<td>Trace Length</td>
<td></td>
<td>Parallel Tx/Rx Length</td>
</tr>
<tr>
<td>PCB</td>
<td>Stackup</td>
<td>Stackup</td>
<td>Stackup</td>
</tr>
<tr>
<td></td>
<td>Trace Length</td>
<td></td>
<td>Parallel Tx/Tx Length</td>
</tr>
<tr>
<td></td>
<td>Dielectric Material</td>
<td>Vias</td>
<td>Layer Changes</td>
</tr>
<tr>
<td>Connector</td>
<td></td>
<td></td>
<td>Footprint Voiding</td>
</tr>
<tr>
<td>Cable</td>
<td>Wire Length</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Wire Gauge</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EMC/RFI</td>
<td>ESD Protection</td>
<td></td>
<td>Common Mode Choke</td>
</tr>
</tbody>
</table>
Typical Routing Configuration
Type C PCB routing estimates

<table>
<thead>
<tr>
<th></th>
<th>Gen 1 (10G)</th>
<th>Gen 2 (10G)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Loss Budget</td>
<td>6.5dB @ 2.5GHz</td>
<td>8.5dB @ 5GHz</td>
</tr>
<tr>
<td>USB 3.1 only</td>
<td>5.5” – 6.5”</td>
<td>5.0” – 6.0”</td>
</tr>
<tr>
<td>USB 3.1 + discrete alt mode mux</td>
<td>4.0” – 5.0”</td>
<td>3.0” – 4.0”</td>
</tr>
<tr>
<td>USB 3.1 + integrated alt mode mux</td>
<td>5.5” – 6.5”</td>
<td>5.0” – 6.0”</td>
</tr>
</tbody>
</table>

Notes

• Loss budgets are for host/device from silicon to port connector.
• These are estimates only. Work with your supplier to determine actual supported length.
• Estimates assume
  ▪ silicon pad cap, jitter & swing at WC recommended/allowed by spec.
  ▪ direct route on PCB from package to Type C™ receptacle.
  ▪ integrated mux has no significant impact on silicon pad cap.
• Actual lengths also depend upon silicon (swing, jitter, EQ, pad cap), package (loss, impedance, crosstalk) and PCB materials.
Impact of Type C Alternate Modes

• Designs with USB Type C may need MUX for:
  • flippability
  • switching between USB 3.1 and alternate modes
• MUX loss ~1.5dB
  • Reduces max length by ~1dB/inch.
  • Discrete MUX makes it more likely you will need a repeater.
  • Opportunity to integrate mux and redriver
Extending Your Reach

- Low Loss PCB Materials
- Internal Cables
- Repeaters
Low Loss PCB Materials

- Using low loss dielectrics in your PCB can cut the differential insertion loss in half compared to conventional FR4 PCBs.
- Don’t forget about the other factors (e.g. pad cap, package loss).

<table>
<thead>
<tr>
<th>Material</th>
<th>df</th>
<th>Loss @ 5GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>FR4</td>
<td>0.0150</td>
<td>0.92-0.95 dB/in</td>
</tr>
<tr>
<td>Low Loss</td>
<td>0.0033</td>
<td>0.48-0.52 dB/in</td>
</tr>
</tbody>
</table>
Low Loss PCB Materials

Low-loss PCB improves Tx compliance margin, providing up to 3” added length.
Internal cable topology

**Approach:** extend reach by using a long internal cable with a short PCB route.

Often used types:
- **Microcoax cable up to 18”**
  - Cable loss ~1/10th of PCB loss
- **FPC/FFC up to 5”**
  - Cable loss ~ PCB loss
Example Cabled Configuration

Controller
BO
M1
Via
M2
Internal cable header

Internal cable header
M3
ESD
M4
USB Connector

Short Stub length

Controller
BO
M1
Internal cable header

Internal cable header
M3
ESD
M4
USB Connector

Short Stub length
Re-timers

- Work with your supplier to determine specific route lengths for your design.
- Re-drivers require additional engineering with supplier to “tune” settings.
- Re-timers can be tested for electrical compliance to the spec.

Estimated PCB route lengths.
Example Re-driver Configuration
PCB Routing Estimates with Repeaters

<table>
<thead>
<tr>
<th>Type C™ Systems</th>
<th>Baseline</th>
<th>Best Case</th>
<th>w/ Re-driver</th>
<th>w/ Re-timer</th>
</tr>
</thead>
<tbody>
<tr>
<td>SS Gen 1 5Gbps Insertion Loss Budget</td>
<td>6.5dB</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gen 1</td>
<td>5.5”</td>
<td>6.5”</td>
<td>&gt;15”</td>
<td></td>
</tr>
<tr>
<td>Gen 1 + DP 1.2 discrete MUX</td>
<td>4.0”</td>
<td>5.0”</td>
<td>&gt;15”</td>
<td></td>
</tr>
<tr>
<td>SS Gen 2 10Gbps Insertion Loss Budget</td>
<td>8.5dB</td>
<td>(+10dB)</td>
<td>(+23dB)</td>
<td></td>
</tr>
<tr>
<td>Gen 2</td>
<td>5.0”</td>
<td>6.0”</td>
<td>11”</td>
<td>&gt;20”</td>
</tr>
<tr>
<td>Gen 2 + DP 1.2 discrete MUX</td>
<td>3.0”</td>
<td>4.0”</td>
<td>9.5”</td>
<td></td>
</tr>
</tbody>
</table>

1. Actual lengths depend upon Tx, Rx, MUX, packages, and PCB materials.
2. Assumes 1.5dB MUX loss & 1dB/in PCB loss @ 5GHz.
3. Baseline estimated assuming spec Tx & Rx. Best case estimated assuming “better than spec” Tx & Rx.
4. Assumes re-driver supports additional 10dB @ 5GHz; re-timer breaks system into two links.
# Re-drivers and Re-timers

<table>
<thead>
<tr>
<th>Benefits</th>
<th>Limitations</th>
</tr>
</thead>
<tbody>
<tr>
<td>Re-driver</td>
<td>Re-timer</td>
</tr>
<tr>
<td>- extend channel by cancelling ISI from channels &amp; amplifying the signal</td>
<td>- extend channel by breaking into multiple links (add up to 23dB),</td>
</tr>
<tr>
<td>- lower cost than re-timers</td>
<td>- supported by spec (Appendix E)</td>
</tr>
<tr>
<td>- zero delay</td>
<td>- protocol aware for better link power management</td>
</tr>
<tr>
<td>- may compensate for ~10dB of additional loss (design dependent)</td>
<td>- ease of integration – standard alone compliance</td>
</tr>
<tr>
<td>- needs to be linear system for ISI to be effectively cancelled</td>
<td>- Added cost if requires a reference clock</td>
</tr>
<tr>
<td>- does not reset jitter</td>
<td>- may consume more power than re-driver in U0</td>
</tr>
<tr>
<td>- no provision for training the receiver EQ – requires tuning to your design</td>
<td>- limited in LPM</td>
</tr>
<tr>
<td>- limited in LPM</td>
<td>- not supported by the spec &amp; no component-level compliance testing</td>
</tr>
<tr>
<td>- not supported by the spec &amp; no component-level compliance testing</td>
<td></td>
</tr>
</tbody>
</table>

Lower cost, limited performance, intensive design

Higher cost, easier integration, better interop
Repeater Comparison

**Benefits**

**Re-drivers**
- extends channel by cancelling ISI from channels & amplifying the signal
- lower cost than re-timers
- zero delay

**Limited to ~10dB of additional loss (design dependent)**
- needs to be linear system for effective ISI cancellation
- does not reset jitter
- no provision for receiver EQ training – requires tuning to your design
- limited link power management
- not supported by the spec & no component-level compliance testing

**Re-timers**
- extends channel by breaking into multiple links (add up to 23dB),
- supported by spec (Appendix E)
- protocol aware for better link power management
- ease of integration – component level compliance

**Limitations**

- added cost if requires a reference clock
- may consume more power than re-driver in U0

**Lower cost, limited performance, intensive design**

- Higher cost, easier integration, better interop
Watch Out For

- Thin PCBs
- PCB Vias
- Connectors
- Crosstalk Minimization
Thin PCBs

Small, light, thin products are driving reduced PCB thicknesses.

- Thinner layers throughout the stackup.
- Potential large reduction in center prepreg
  - Refer to the example 6 layer stackup

<table>
<thead>
<tr>
<th>Layer</th>
<th>Function</th>
<th>Material</th>
<th>&quot;Standard&quot; PCB</th>
<th>&quot;Thin&quot; PCB</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Signal / PWR</td>
<td>0.5oz + Plating</td>
<td>1.8</td>
<td>1.8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Pre Preg</td>
<td>2.8</td>
<td>2.0</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>1oz</td>
<td>1.2</td>
<td>0.6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CORE</td>
<td>3.9</td>
<td>2.0</td>
</tr>
<tr>
<td>3</td>
<td>Signal / PWR</td>
<td>1oz</td>
<td>1.2</td>
<td>0.6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Pre Preg</td>
<td>21.7</td>
<td>11.0</td>
</tr>
<tr>
<td>4</td>
<td>Signal</td>
<td>1oz</td>
<td>1.2</td>
<td>0.6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CORE</td>
<td>3.9</td>
<td>2.0</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>1oz</td>
<td>1.2</td>
<td>0.6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Pre Preg</td>
<td>2.8</td>
<td>2.0</td>
</tr>
<tr>
<td>6</td>
<td>Signal / PWR</td>
<td>0.5oz + Plating</td>
<td>1.8</td>
<td>1.8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Solder Mask</td>
<td>0.5</td>
<td>0.5</td>
</tr>
</tbody>
</table>

TOTAL: 44.3 vs 25.8
Reducing dielectric thickness ($D_2$) to <11mils impacts electrical performance metrics:

- Similar impedance ($Z_{\text{diff}}$) & loss ($A$)
- Reduced intra-layer crosstalk ($K_{b1}$, $K_{f1}$)
- Increased layer-layer crosstalk ($K_{b2}$, $K_{f2}$)
PCB Vias: Impact

Via stubs cause reflections that reduce design margins.
PCB Vias: Stub Mitigation

Keep via stub < 15mil

<table>
<thead>
<tr>
<th>8-Layer Stackup</th>
<th>Thickness (mil)</th>
<th>Exit Stub Length (mil)</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1 Trace</td>
<td>1.9</td>
<td></td>
</tr>
<tr>
<td>FR4_1080</td>
<td>2.7</td>
<td></td>
</tr>
<tr>
<td>L2 Plane</td>
<td>1.3</td>
<td></td>
</tr>
<tr>
<td>FR4_2116</td>
<td>4</td>
<td>~50</td>
</tr>
<tr>
<td>L3 Trace</td>
<td>1.3</td>
<td>~10</td>
</tr>
<tr>
<td>FR4_7628</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>L4 Plane</td>
<td>2.6</td>
<td></td>
</tr>
<tr>
<td>FR4_2116</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>L5 Plane</td>
<td>2.6</td>
<td></td>
</tr>
<tr>
<td>FR4_7628</td>
<td>4.2</td>
<td></td>
</tr>
<tr>
<td>L6 Trace</td>
<td>1.3</td>
<td>~10</td>
</tr>
<tr>
<td>FR4_2116</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>L7 Plane</td>
<td>1.3</td>
<td></td>
</tr>
<tr>
<td>FR4_1080</td>
<td>2.7</td>
<td></td>
</tr>
<tr>
<td>L8 Trace</td>
<td>1.9</td>
<td></td>
</tr>
<tr>
<td>Solder Mask</td>
<td>0.65</td>
<td></td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>62.9</strong></td>
<td></td>
</tr>
</tbody>
</table>

Increase antipad size

<table>
<thead>
<tr>
<th>Color</th>
<th>Antipad diameter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Red</td>
<td>30 mil</td>
</tr>
<tr>
<td>Blue</td>
<td>40 mil</td>
</tr>
<tr>
<td>Green</td>
<td>50 mil</td>
</tr>
<tr>
<td>Cyan</td>
<td>60 mil</td>
</tr>
<tr>
<td>Purple</td>
<td>70 mil</td>
</tr>
</tbody>
</table>

Superspeed USB 10Gbps

USB Developer Days – October 19 – 20, 2016

ShenZhen Legendary USB Implementers Forum © 2016
Connectors: Guideline for Type C™ Footprint Voiding

**SMT Ground void**
- L: Ground void length
- W: Ground void width

**PTH Ground Void**
- a: Finished hole radius
- b: Annular ring radius
- R: Antipad radius to PTH center
- P: Antipad center to center distance

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>a  finished hole radius</td>
<td>0.40mm</td>
</tr>
<tr>
<td>b  annular ring radius</td>
<td>0.65mm</td>
</tr>
<tr>
<td>R  antipad radius to PTH center</td>
<td>1.00mm</td>
</tr>
<tr>
<td>P  antipad center to center distance</td>
<td>0.8mm</td>
</tr>
</tbody>
</table>
**PCB Crosstalk Minimization**

**Recommendation:** Breakout Tx and Rx I/O on different PCB layers.

- Non-interleaved routing.
  - Eliminates a key source of near end crosstalk.

- Places requirements on Tx & Rx I/O placement as shown to the left.

- Note that package is also a source of crosstalk.
  - Refer to the “USB 3.1 System Design” presentation from November 2015.

Board surface layer:
- **Tx BGAs** at outer region
- Breakout as Microstrip

Board inner layer:
- **Rx BGAs** at inner region
- Breakout as Stripline
Summary

• Your 10G USB 3.1 designs may have reduced PCB trace lengths:
  ▪ Loss, reflections & crosstalk
  ▪ Discrete mux for Type C™ alternate modes

• You have options for supporting longer lengths:
  ▪ Low loss PCBs
  ▪ Internal cabling
  ▪ Repeaters

• Exercise care in dealing with:
  ▪ Thin PCBs
  ▪ PCB vias
  ▪ Connector footprint optimization
  ▪ PCB crosstalk
Q&A Session